

01 智能建库工具



PART

1-1. 结合OCR丰富的算法

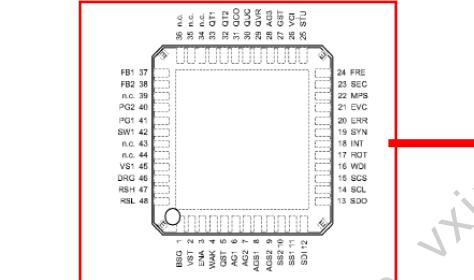
根据芯片设计图纸，从中萃取出芯片的PIN脚信息。以便建库及检查。



Infineon TLF35584 Pin Configuration

3 Pin Configuration

3.1 Pin Assignment - PG-VQFN-48



Figures 2 Pin Configuration - PG-VQFN-48

3.2 Pin Definitions and Functions - PG-VQFN-48

Pin	Symbol	Function
1	BSG	Boost driver ground: Connect this pin to ground at the low side of an external current sense resistor to decouple the driver noise from the sensitive ground. If step up pre regulator option is not used, connect to ground.
2	VST	Supply voltage standby regulator input: Connect this input to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
3	ENA	Enable input: A positive edge signal at this pin will wake the device. In case of not used connect to ground.
4	WAK	Wake/Inhibit Input: A high level signal of defined length at this pin will wake the device. In case of not used, connect to ground.

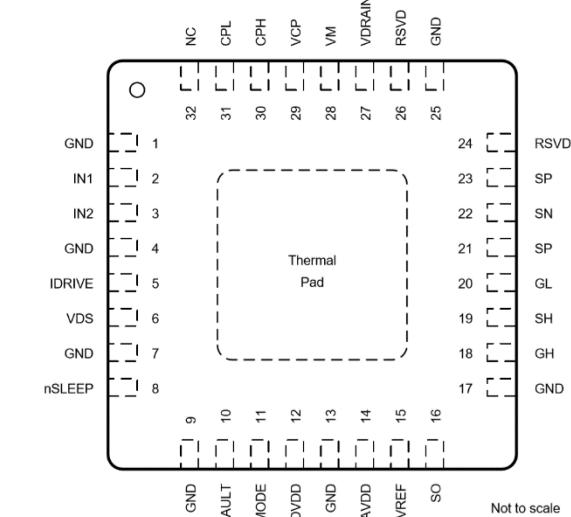
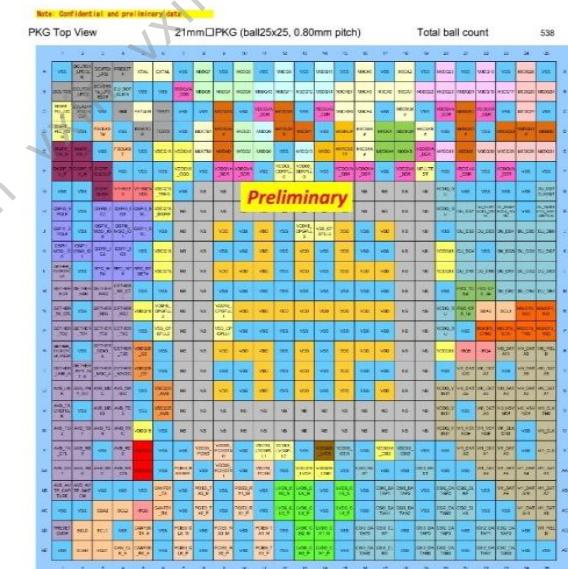
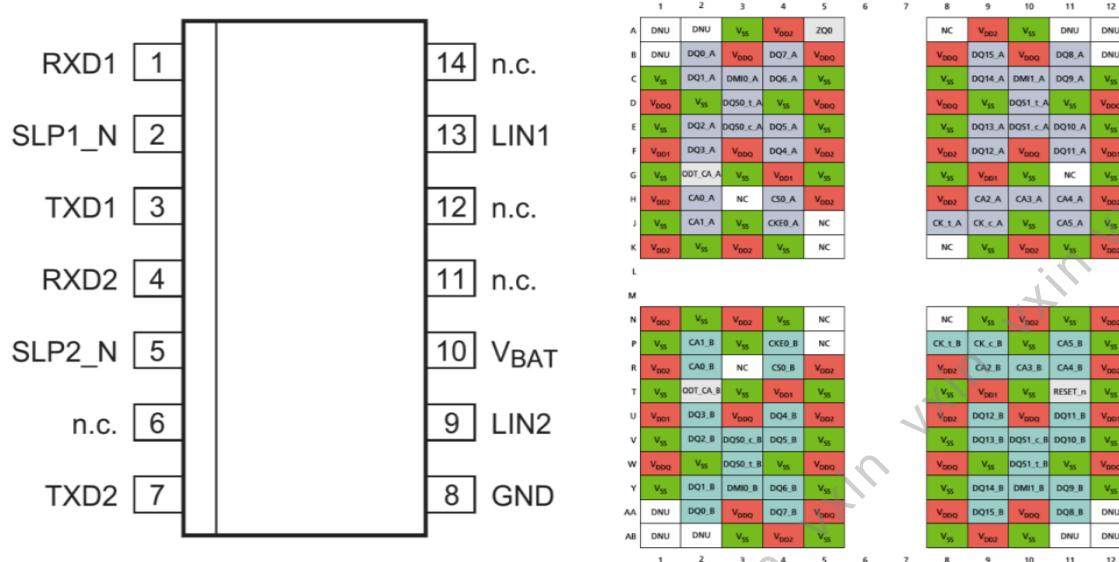
Data Sheet 8 Rev. 2.0, 2017-03-16 copy to PATAc

信息萃取

PIN	PIN脚信息
1	BSG
2	VST
3	ENA
4	WAK
5	QST
...	...

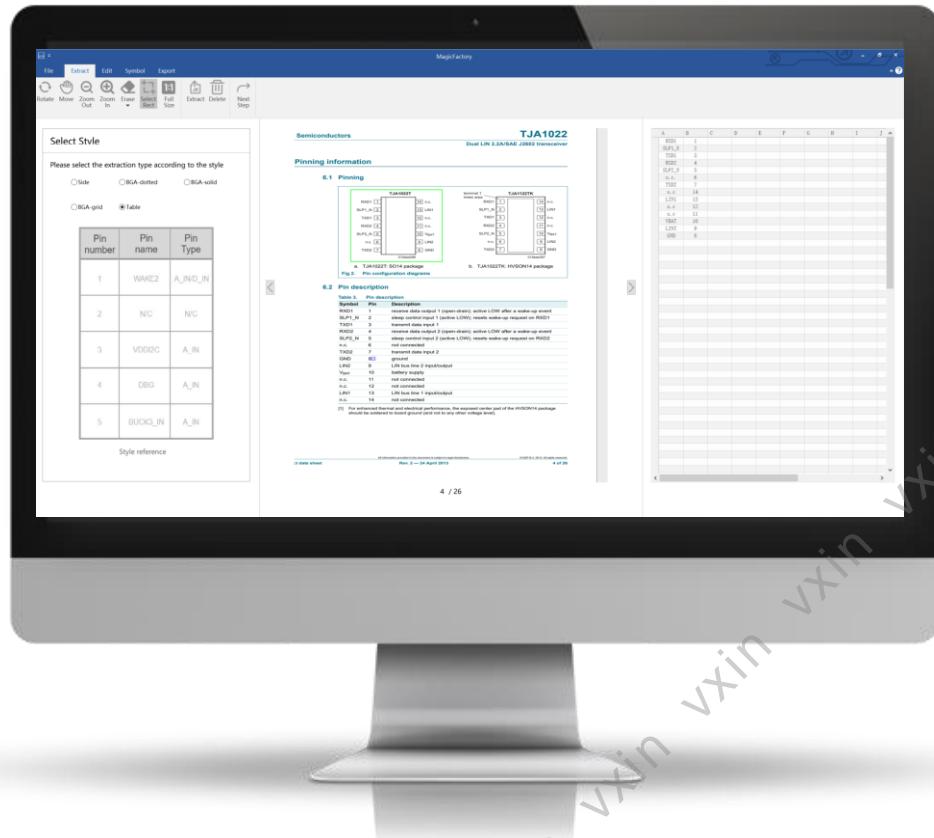
第一次将AI引入EDA

支持数据类型：两边出脚、四边出脚、表格格式（框线清晰）、BGA矩阵格式，萃取出Pin Name、Pin Number信息。



第一步 智能识别

无论什么规格说明书，在这里，一秒变成文字！



功能优势

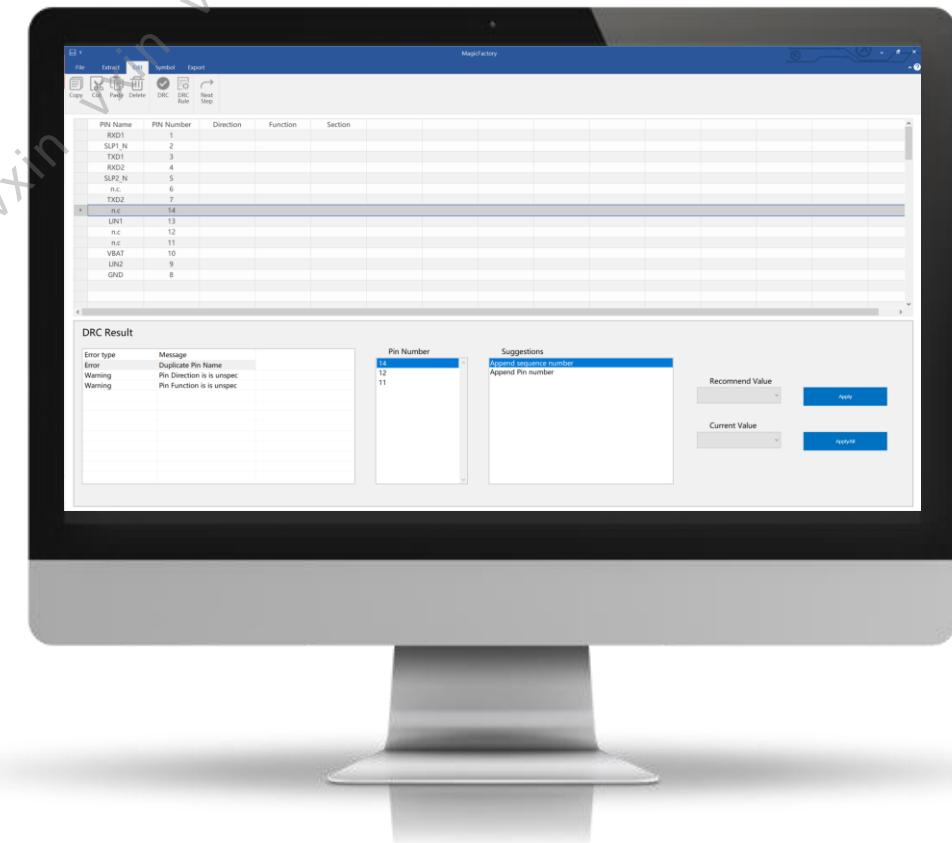
- 识别SOP、QFP、BGA等多种类型
- 支持萃取Pin Number、Name等多种信息
- 支持二级管、三极管等非标格式
- 可定位和识别不规则文字

第二步 信息优化

PIN脚信息不全？数量太多一个个太难改？别怕，这里直接一键补全！

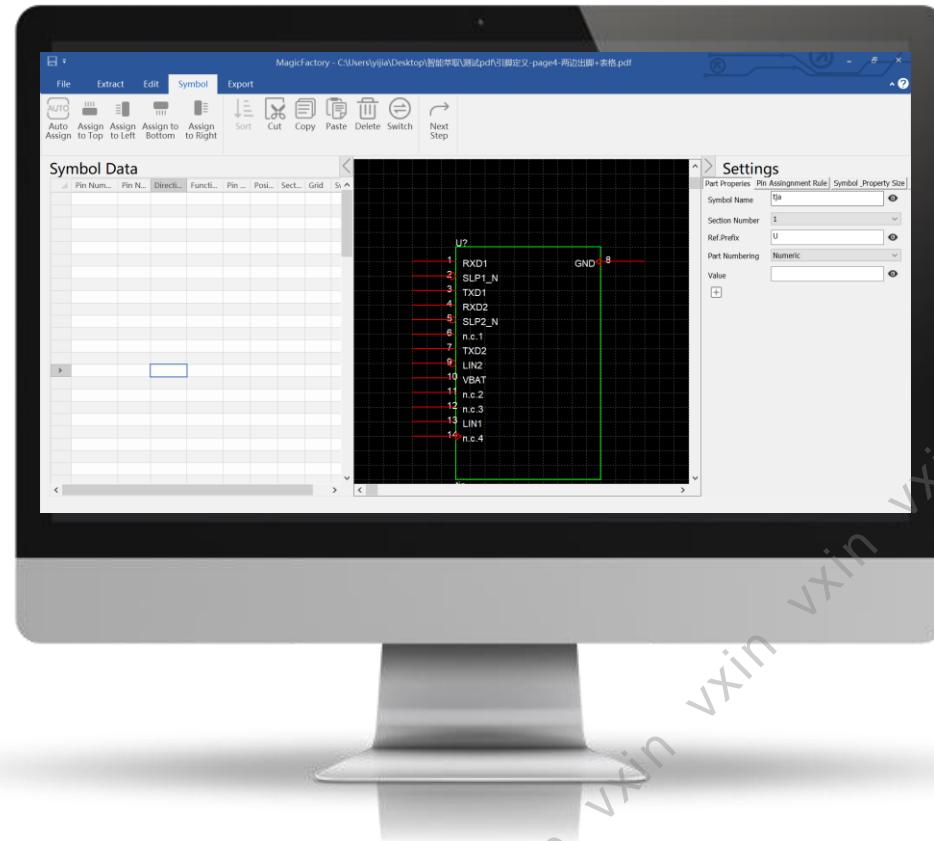
功能优势

- Pin Type识别及自动推荐类型
- 自动识别低电平有效等特殊电气属性
- 可编辑引脚信息，优化Pin Function
- 自动编号重复的Pin Name



第三步 智能建库

就算是一千个PIN脚又怎样呢，手指点一下，乖乖摆布到元件上！

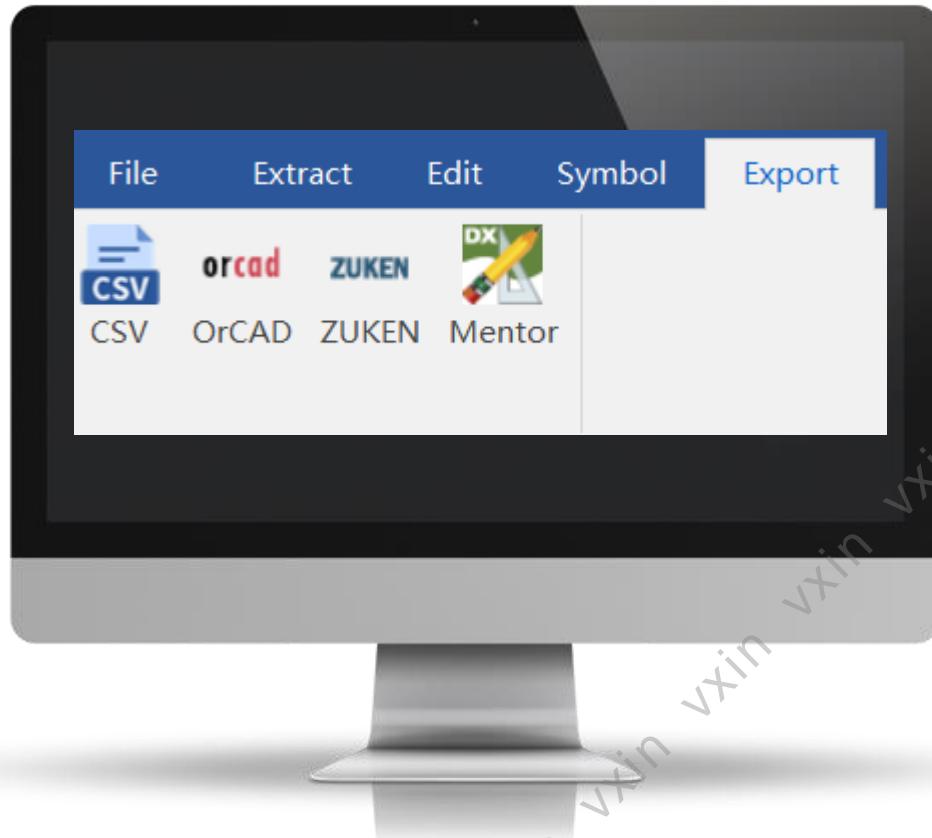


功能优势

- 支持手动排布任意引脚
- 支持单个或一组引脚拖拽摆放
- 依据Pin Type属性自动排布引脚位置
- 支持编辑symbol图框大小
- 支持自定义symbol属性参数

第四步 输出建库

自动导出多种EDA工具原理图符号库



功能优势

- 支持输出Cadence OrCAD原理图符号库
- 支持输出Zuken Design Gateway原理图符号库
- 支持输出Mentor EPD原理图符号库
- 支持输出CSV 格式pin 引脚信息表

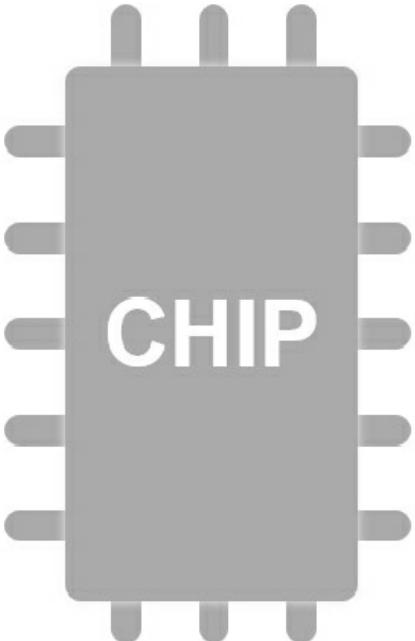
四边出脚类型Pin Map萃取

萃取结果24 pins

Select Style

Please select the extraction type according to the style

- Side2 BGA-dotted BGA-solid
 BGA-grid Table Side4

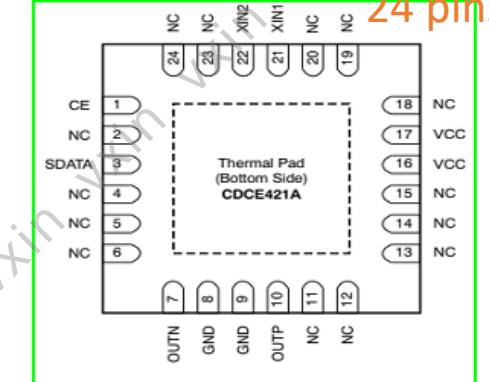


Style reference

TEXAS INSTRUMENTS **CDCE421A**
www.ti.com SCAS873-1

DEVICE INFORMATION

RGE PACKAGE
QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

Table 1. CDCE421A Pin Descriptions

TERMINAL NAME	TERMINAL NO.	TYPE	ESD PROTECTION	DESCRIPTION
CE	1	I	Y	Chip enable CE = 1: enable the device and the outputs. CE = 0: disable all current sources; in LVDS mode, LVDSP = LVDS in LVPECL mode, LVPECL = LVPECLN = Hi-Z.
GND	8, 9	GND	Y	Ground
No connect	2, 4-6, 11-15, 18-20, 23, 24			Do not connect these pins. Leave them floating.
OUTN	7	O	Y	High-speed negative differential LVPECL or LVDS outputs. (Outputs enabled by CE and selected by the EEPROM configuration registers.)
OUTP	10	O	Y	High-speed positive differential LVPECL or LVDS outputs. (Outputs enabled by CE and selected by the EEPROM configuration registers.)
SDATA	3	I	Y	Programming pin using TI proprietary interface protocol
VCC	16, 17	Power	Y	3.3-V power supply
XIN1 XIN2	21 22	I GND/NC	Y N	In crystal input mode, connect XIN1 to one end of the crystal and XIN2 other end of the crystal. In LVCMS input single-ended driven mode (pin 21) acts as an input reference, and XIN2 should connect to GND be left unconnected.

	B	C
1	1	CE
2	2	NC
3	3	SDATA
4	4	NC
5	5	NC
6	6	NC
7	7	OUTN
8	8	GND
9	9	GND
10	10	OUTP
11	11	NC
12	12	NC
13	13	NC
14	14	NC
15	15	NC
16	16	Vcc
17	17	Vcc
18	18	NC
19	19	NC
20	20	NC
21	21	XIN1
22	22	XIN2
23	23	NC
24	24	NC
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		

Select Style

Please select the extraction type according to the style

Side2 BGA-dotted BGA-solid

BGA-grid Table Side4

1	2	3	4	5	6	7	8		A	B	C	D	E	F	G	H	I	J	K	L
A									A	B	C	D	E	F	G	H	I	J	K	L

Style reference

Data Sheet AD9208

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9208

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVDD2	AVDD2	AVDD1	AVDD1 ¹	AVDD1 ¹	AGND ¹	CLK+	CLK-	AGND ¹	AVDD1 ¹	AVDD1 ¹	AVDD1	AVDD2	AVDD2
B	AVDD2	AVDD2	AVDD1	AVDD1 ¹	AGND	AGND ¹	AGND ¹	AGND ¹	AGND ¹	AGND	AGND	AVDD1	AVDD2	AVDD2
C	AVDD2	AVDD2	AVDD1	AGND	AGND	AGND ¹	AGND ¹	AGND ¹	AGND	AGND	AGND	AVDD1	AVDD2	AVDD2
D	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND ¹	AGND ¹	AGND	AGND	AGND	AGND	AGND	AVDD3
E	VIN-B	AGND	AGND	AGND	AGND	AGND ²	AVDD1_SR	AGND ²	AGND	AGND	AGND	AGND	AGND	VIN-A
F	VIN+B	AGND	AGND	AGND	AGND	AGND	SYSREF+-	SYSREF--	AGND	AGND	AGND	AGND	AGND	VIN+A
G	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3
H	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	VREF	AGND	AGND	AGND	AGND	AGND
J	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
K	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³	AGND ³
L	DGND	GPIO_B1	SPIVDD	FD_B/ GPIO_B2	CSB	SCLK	SDIO	PDOWN/ STBY	FD_A/ GPIO_A2	SPIVDD	GPIO_A1	DGND	DGND	DGND
M	DGND	DGND	DGND	DGND	DRVDD1	DRVDD1	DRVDD1	DRVDD1	DGND	DGND	DRVDD1	DRVDD1	DRVDD2	DVDD
N	DVDD	DVDD	DGND	SERDOUT ⁴	DGND	SYNCINB+	DVDD							
P	DVDD	DVDD	DGND	SERDOUT ⁵	DGND	SYNCINB-	DVDD							

*DENOTES CLOCK DOMAIN.
^DENOTES SYSREF DOMAIN.
^DENOTES ISOLATION DOMAIN.

Figure 5. Pin Configuration (Top View)

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A	B	C
166	M12	DRGND
167	M13	DRVDD2
168	M14	DVDD
169	N1	DVDD
170	N2	DVDD
171	N3	DRGND
172	N4	SERDOUT7+
173	N5	SERDOUT6+
174	N6	SERDOUT5+
175	N7	SERDOUT4+
176	N8	SERDOUT3+
177	N9	SERDOUT2+
178	N10	SERDOUT1+
179	N11	SERDOUT0+
180	N12	DRGND
181	N13	SYNCINB+
182	N14	DVDD
183	P1	DVDD
184	P2	DVDD
185	P3	DRGND
186	P4	SERDOUT7-
187	P5	SERDOUT6-
188	P6	SERDOUT5-
189	P7	SERDOUT4-
190	P8	SERDOUT3-
191	P9	SERDOUT2-
192	P10	SERDOUT1-
193	P11	SERDOUT0-
194	P12	DRGND
195	P13	SYNCINB-
196	P14	DVDD
197		
198		
199		

完美去除水印



UG51U6400N8SU-ACF

PIN CONFIGURATIONS

204-Pin DDR3 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	
1	V _{REFDQ}	53	DQ19	105	V _{DD}	157	DQ42
3	V _{SS}	55	V _{SS}	107	A10	159	DQ43
5	DQ0	57	DQ24	109	BA0	161	V _{SS}
7	DQ1	59	DQ25	111	V _{DD}	163	DQ48
9	V _{SS}	61	V _{SS}	113	WE#	165	DQ49
11	DM0	63	DM3	115	CAS#	167	V _{SS}
13	V _{SS}	65	V _{SS}	117	V _{DD}	169	DQS6#
15	DQ2	67	DQ26	119	A13	171	DQS6
17	DQ3	69	DQ27	121	S1#	173	V _{SS}
19	V _{SS}	71	V _{SS}	123	V _{DD}	175	DQ50
21	DQ8	73	CKE0	125	NC	177	DQ51
23	DQ9	75	V _{DD}	127	V _{SS}	179	V _{SS}
25	V _{SS}	77	NC	129	DQ32	181	DQ56
27	DQS1#	79	BA2	131	DQ33	183	DQ57
29	DQS1	81	V _{DD}	133	V _{SS}	185	V _{SS}
31	V _{SS}	83	A12	135	DQS4#	187	DM7
33	DQ10	85	A9	137	DQS4	189	V _{SS}
35	DQ11	87	V _{DD}	139	V _{SS}	191	DQ58
37	V _{SS}	89	A8	141	DQ34	193	DQ59
39	DQ16	91	A5	143	DQ35	195	V _{SS}
41	DQ17	93	V _{DD}	145	V _{SS}	197	SA0
43	V _{SS}	95	A3	147	DQ40	199	V _{DDSPD}
45	DQS2#	97	A1	149	DQ41	201	SA1
47	DQS2	99	V _{DD}	151	V _{SS}	203	V _{TT}
49	V _{SS}	101	CK0	153	DM5		
51	DQ18	103	CK0#	155	V _{SS}		

自动消除水印

萃取结果

	D	E	F	G	H	I
1	53	DQ19	105	VDD	157	DQ42
2	55	VSS	107	A10	159	DQ43
3	57	DQ24	109	BA0	161	VSS
4	59	DQ25	111	VDD	163	DQ48
5	61	VSS	113	WE#	165	DQ49
6	63	DM3	115	CAS#	167	VSS
7	65	VSS	117	VDD	169	DQS6#
8	67	DQ26	119	A13	171	DQS6
9	69	DQ27	121	S1#	173	VSS
10	71	VSS	123	VDD	175	DQ50
11	73	CKE0	125	NC	177	DQ51
12	75	VDD	127	VSS	179	VSS
13	77	NC	129	DQ32	181	DQ56
14	79	BA2	131	DQ33	183	DQ57
15	81	VDD	133	VSS	185	VSS
16	83	A12	135	DQS4#	187	DM7
17	85	A9	137	DQS4	189	VSS
18	87	VDD	139	VSS	191	DQ58
19	89	A8	141	DQ34	193	DQ59
20	91	A5	143	DQ35	195	VSS
21	93	VDD	145	VSS	197	SA0
22	95	A3	147	DQ40	199	V _{DDSPD}
23	97	A1	149	DQ41	201	SA1
24	99	VDD	151	VSS	203	VTT
25	01	CK0	153	DM5		
26	03	CK0#	155	VSS		
27						
28						
29						